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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,320	08/21/2003	Jeff Raynor	02ED04552629	7555
27975	7590	02/24/2005	EXAMINER	
ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.			HUYNH, ANDY	
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE				
P.O. BOX 3791			ART UNIT	PAPER NUMBER
ORLANDO, FL 32802-3791			2818	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/645,320	Applicant(s) RAYNOR, JEFF	
	Examiner Andy Huynh	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14-51 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 14-19, 21, 22, 25, 29-33, 35, 36, 39, 43-45 and 47-49 is/are rejected.
- 7) ☒ Claim(s) 20, 23, 26-28, 34, 37, 38, 40-42, 46, 50 and 51 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

In the Amendment dated January 27, 2005, claims **1-13** are canceled, and claims **14, 29** and **43** are amended is acknowledged. Accordingly, claims **14-51** remain pending in this application.

Response to Arguments

Applicant's arguments, see the Amendment, filed 01/27/2005, with respect to the rejection(s) of claim(s) **14-19, 21, 22, 25, 29-33, 35, 36, 39, 43-45 and 47-49** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **14-19, 21, 22, 25, 29-32, 33, 35, 36, 39, 43-45 and 47-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1-2 of Prior Art, Applicant's admitted prior arts (AAPA), in view of Watanabe (USP 6,448,104).

Regarding claims **14 and 15**, Figs. 1-2 of Prior Art (AAPA) and the corresponding texts as set forth in paragraphs [0018]-[0022] disclose a solid state image sensor comprises:

a substrate 10 of a first conductivity type P-type;
an epitaxial layer 12 of the first conductivity type on said substrate; and
an active pixel array said epitaxial layer, each pixel comprising
a first well 14 of a second conductivity type N-type functioning as a collection
node, and
at least one second well 16 the first conductivity type adjacent said first well, and
a plurality of MOS transistors of the second conductivity type NMOS functioning as
active elements of said pixel.

Figs. 1-2 of AAPA fail to teach the solid-state image sensor comprises a plurality of MOS transistors of only the second conductivity type. Watanabe discloses in Fig. 3C and the corresponding texts as set forth in col. 7, line 39-col. 9, line 21, a solid imaging device comprises a plurality of MOS transistors of only the second conductivity type N-type 131. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a solid imaging device comprising a plurality of MOS transistors of only the second conductivity type N-type, as taught by Watanabe to incorporate into and modify Figs. 1-2 of AAPA to arrive the claimed limitation to be operable to amplify a level of a signal from the photosensitive portion (col. 5, lines 22-30).

Regarding claims 16, 30 and 31, Figs. 1-2 of Prior Art and Watanabe disclose the claimed limitations except for a solid state image sensor wherein the first conductivity type comprises an N-type conductivity, and the second conductivity type comprises P-type conductivity; wherein said substrate is of the second conductivity type, and wherein the first conductivity type comprises type conductivity and the second conductivity type comprises an N-

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type conductivity; and wherein said substrate is of the first conductivity type; and wherein the first conductivity type comprises type conductivity and the second conductivity type comprises P-type conductivity. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the first conductivity type comprises an N-type or P-type conductivity, and the second conductivity type comprises P-type or N-type conductivity since it was known in the art that it could be inverted by reversing the polarity of the conductivity.

Regarding claims **17-19, 44 and 45**, Figs. 1-2 of Prior Art (AAPA) disclose a solid state image sensor further comprising circuit elements external said active pixel array, and wherein said active elements each pixel and said external circuit elements form part of an analog-to-digital converter; further comprising least one comparator external said active pixel array and wherein said active elements in each pixel form an amplifier connected to said at least one comparator for forming part of the analog-to-digital converter; and wherein said active elements in each pixel are selectively switched to said at least one comparator.

Regarding claims **21, 22, 35, 36, 47 and 48**, Figs. 1 and 2 of Prior Art (AAPA) disclose a solid state image sensor further comprising a latch connected to said at least one comparator in which a count is latched by a change of state of said at least one comparator; and further comprising a frame store circuit connected to said latch for receiving the count latched by said latch.

Regarding claims **25, 39 and 49**, Figs. 1 and 2 of Prior Art (AAPA) disclose a solid state image sensor a solid state image sensor further comprising circuit elements external said active pixel array, said external circuit elements comprising respective comparator and counter for each pixel.

Regarding claim **29**, Figs. 1 and 2 of Prior Art (AAPA) and the corresponding texts as set forth in paragraphs [0018]-[0022] disclose a solid state image sensor comprises:

a substrate 10;

an active pixel array in said substrate, each pixel comprising

a first well 14 of a first conductivity type N-type functioning as a collection node,

and

at least one second well 16 of a second conductivity type P-type adjacent said first well, and comprising a plurality of MOS transistors of the first conductivity type NMOS functioning as active elements; and

circuit elements in said substrate and external said active pixel array and forming analog-to-digital converters with the active elements therein.

Figs. 1-2 of AAPA fail to teach the solid-state image sensor comprises a plurality of MOS transistors of only the second conductivity type. Watanabe discloses in Fig. 3C and the corresponding texts as set forth in col. 7, line 39-col. 9, line 21, a solid imaging device comprises a plurality of MOS transistors of only the second conductivity type N-type 131. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a solid imaging device comprising a plurality of MOS transistors of only the second conductivity type N-type, as taught by Watanabe to incorporate into and modify Figs. 1-2 of AAPA to arrive the claimed limitation to be operable to amplify a level of a signal from the photosensitive portion (col. 5, lines 22-30).

Regarding claims **32 and 33**, Figs. 1 and 2 of Prior Art (AAPA) disclose a solid state image sensor wherein said circuit elements external each pixel comprise at least one comparator;

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and wherein said active elements in each pixel form an amplifier connected to said at least one comparator for forming an analog-to-digital converter; and wherein said active elements in each pixel are selectively switched to said at least one comparator.

Regarding claim 43, Figs. 1 and 2 of Prior Art (AAPA) and the corresponding texts as set forth in paragraphs [0018]-[0022] disclose a method for making a solid state image sensor comprises:

- forming an active pixel array in a substrate 10, and

- forming each pixel comprising

 - forming a first well 14 of a first conductivity type N-type functioning as collection node, and

 - forming at least one second well 16 of a second conductivity type P-type adjacent the first well, the least one second well comprising a plurality of MOS transistors of the first conductivity type NMOS functioning as active elements; and

- forming circuit elements in the substrate external the active pixel array and forming analog-to-digital converters with the active elements therein.

Figs. 1-2 of AAPA fail to teach the solid-state image sensor comprises a plurality of MOS transistors of only the second conductivity type. Watanabe discloses in Fig. 3C and the corresponding texts as set forth in col. 7, line 39-col. 9, line 21, a solid imaging device comprises a plurality of MOS transistors of only the second conductivity type N-type 131. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a solid imaging device comprising a plurality of MOS transistors of only the second conductivity type N-type, as taught by Watanabe to incorporate into and modify Figs. 1-2 of AAPA to arrive

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the claimed limitation to be operable to amplify a level of a signal from the photosensitive portion (col. 5, lines 22-30).

Allowable Subject Matter

Claims 20, 23-24, 26-28, 34, 37, 38, 40-42, 46, 50 and 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Figs. 1 and 2 of Prior Art fail to teach or suggest a solid state image sensor wherein said circuit elements external each pixel comprise at least one current mirror connected to said at least one comparator; and wherein said active elements in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to said at least one current mirror connected thereto as recited in claim 20; a solid state image sensor further comprising circuit elements external said active pixel array, said external circuit elements comprising comparators and counters, and wherein a number of pixels given row or column of said active pixel array share single comparator and counter, with the corresponding pixels in the given row or column being enabled sequentially as recited in claim 26; a solid state image sensor wherein said circuit elements external each pixel comprise least one current mirror connected to said at least one comparator; and wherein said active elements in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to said at least one current mirror connected thereto as recited in claim 34; a solid state image sensor wherein said circuit elements external each

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pixel further comprise comparators and counters for said active pixel array, and wherein a number of pixels a given row or column of said active pixel array share single comparator and counter, with the pixels being enabled sequentially as recited in claim 40; a method wherein the circuit elements external each pixel comprise at least one current mirror connected to the at least one comparator; and wherein the active elements in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to the at least one current mirror connected thereto as recited in claim 46; and a method wherein the circuit elements external each pixel further comprise comparators and counters for the active pixel array, and wherein a number of pixels in a given row or column the active pixel array share a single comparator and counter, with the pixels being enabled sequentially as recited in claim 50.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

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Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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02/22/05



Andy Huynh

Patent Examiner